Sunday June 22, 2008

6:00p.m. – 8:30p.m. Registration near Grand Ballroom

6:30p.m. – 8:30p.m. Reception in Grand Ballroom (sponsored by IBM Corporation and IBM Research China)

Monday June 23, 2008

All sessions in Grand Ballroom

8:00-8:30 Breakfast

8:30-8:40 Welcome by general and program chairs

8:40-9:40 Keynote: "*Micro-architecture is Dead, Long Live Micro-architecture," Justin Rattner, Chief Technology Officer, Intel*

9:40-10:00 Break 1

10:00-11:30 –Session 1–*Novel Microarchitectures-Part I*

Chair: *David Kaeli, Northeastern University*

Achieving Out-of-Order Performance with Almost In-Order Complexity, Francis Tseng and Yale N. Patt

Fetch-Criticality Reduction through Control-Independence, Mayank Agarwal, Nitin Navale, Kshitiz Malik, and Matthew I. Frank

A two-level Load/Store Queue based on Execution Locality, Miquel Pericàs, Adrian Cristal, Francisco J. Cazorla, Ruben González, Alex Veidenbaum, Daniel A. Jiménez, and Mateo Valero

11:30-1:30 Lunch (Buffet in hotel restaurant)

1:30 - 3:00 Session 2 (Parallel Sessions)

Session 2a *Novel Memory Systems*

Chair: *Hsien-Hsin Lee, Georgia Tech*

Self-Optimizing Memory Controllers: A Reinforcement Learning Approach, Engin İpek, Onur Mutlu, José F. Martínez, and Rich Caruana

A Comprehensive Memory Modeling Tool and Its Application to the Design and Analysis of Future Memory, Shyamkumar Thoziyoor, Jung Ho Ahn, Matteo Monchiero, Jay B. Brockman, and Norman P. Jouppi

Parallelism-Aware Batch Scheduling: Enhancing Both Performance and Fairnessof Shared DRAM, Onur Mutlu and Thomas Moscibroda

Session 2b *Interconnect Networks - Part I*

Chair: *Matthew Frank, UIUC*

Technology-Driven, Highly-Scalable Dragonfly Topology, John Kim, William J. Dally, Steve Scott, and Dennis Abts

Globally-Synchronized Frames for Guaranteed Quality-of-Service in On-Chip Networks, Jae W. Lee, Man Cheuk Ng, and Krste Asanović

Polymorphic On-Chip Networks, Martha Mercaldi Kim, John D. Davis, Mark Oskin, and Todd Austin

3:00-3:30 Break 2

3:30-5:00 Session 3 (Parallel Sessions)

Session 3a –*Transactional Memory*

Chair: *Scott Mahlke, Univ. of Michigan, Ann Arbor*

Using Memory Protection to Build a High-Performance, Strongly Atomic Hybrid Transactional Memory, Lee Baugh, Naveen Neelakantam, and Craig Zilles

TokenTM: Efficient Execution of Large Transactions with Hardware Transactional Memory, Jayaram Bobba, Neelam Goyal, Mark D. Hill, Michael M. Swift,and David A. Wood

Flexible Decoupled Transactional Memory Support, Arrvindh Shriraman, Sandhya Dwarkadas, and Michael L. Scott

Session 3b *Emergent Technology*

Chair: *Zhiwei Xu, ICT, CAS*

Corona: System Implications of Emerging Nanophotonic Technology, Dana Vantrease, Robert Schreiber, Matteo Monchiero, Moray McLaren, Norman P. Jouppi, Marco Fiorentino, Al Davis, Nathan Binkert, Raymond G. Beausoleil, and Jung Ho Ahn

Microcoded Architectures for Ion-Trap Quantum Computers, Lucas Kreger-Stickles and Mark Oskin

Running a Quantum Circuit at the Speed of Data, Nemanja Isailovic, Mark Whitney, Yatish Patel, and John Kubiatowicz

5:00–5:30 Break (Prepare for panel)

5:30–6:45 Panel Session "Computer Architecture Research and ISCA: Have We Lost Our Compass?"

Moderator: *Yale Patt, UT Austin.*

6:45-7:45 Business meeting

Tuesday June 24, 2008

All sessions in Grand Ballroom

8:00-8:30 – Breakfast

8:30-9:30 Keynote: "*10 important problems in Computer Architecture," David Kirk –Chief Scientist, nVidia*

9:30-10:30 Panel Session " Computer Industry in China - Where Is It Going? "

Moderator: *Wen-mei Hwu, UIUC*

Panelists: *Dick Kramlich, G. Partner and Co-Founder, NEA, Guojie Li, Director, ICT, CAS, Songde Ma, former vice-minister, Ministry of Sci.& Tech, Wen-Hann Wang, Vice President, Intel, Wei Wei, Executive Vice President, Lenovo Research Institute.*

10:30 – 12:00 Award luncheon (Sponsored by Microsoft Corporation and Microsoft Research Asia)

12:00 – 1:00 (prepare room for parallel sessions)

1:00 - 2:30 Session 4 (Parallel Sessions)

Session 4a *Novel Microarchitectures - Part II*

Chair: *Uri Weiser, Technion & Commex*

ReVIVaL: A Variation-Tolerant Architecture Using Voltage Interpolation and Variable Latency, Xiaoyao Liang, Gu-Yeon Wei, and David Brooks

Trading Off Cache Capacity for Reliability to Enable Low Voltage Operation, Chris Wilkerson, Hongliang Gao, Alaa R. Alameldeen, Zeshan Chishti, Muhammad Khellah, and Shih-Lien Lu

Counting Dependence Predictors, Franziska Roesner, Doug Burger, and Stephen W. Keckler

Session 4b *Interconnect Networks - Part II*

Chair: *Onur Mutlu, Microsoft Research*

Virtual Circuit Tree Multicasting: A Case for On-Chip Hardware Multicast Support, Natalie Enright Jerger, Li-Shiuan Peh, and Mikko Lipasti

iDEAL: Inter-Router Dual-function Energy and Area-efficient Links for Network-on-Chip (NoC) Architectures, Avinash Karanth Kodi, Ashwini Sarathy, and Ahmed Louri

MIRA: A Multi-layer On Chip Interconnect Router Architecture, Dongkook Park, Soumya Eachempati, Reetuparna Das, Asit K. Mishra, Yuan Xie, N. Vijaykrishnan, and Chita R. Das

2:30-3:00 Break 3

3:00-4:30 Session 5 (Parallel Sessions)

Session 5a *Debugging Parallel Programs*

Chair: *Xiaowei Shen, IBM Research*

Rerun: Using Episodes for Lightweight Race Recording, Derek R. Hower and Mark D. Hill

Atom-Aid: Detecting and Surviving Atomicity Violations, Brandon Lucia, Joseph Devietti, Karin Strauss, and Luis Ceze

Recording and Deterministically Replaying Shared-Memory Multiprocessor Execution Efficiently, Pablo Montesinos, Luis Ceze, and Josep Torrellas

Session 5b *System Architecture and I/O*

Chair: *Nathan Clark, Georgia Tech*

Intra-Disk Parallelism: An Idea Whose Time Has Come, Sriram Sankar, Sudhanva Gurumurthi, and Mircea R. Stan

Understanding and Designing New Server Architectures for Emerging Warehouse-Computing Environments, Kevin Lim, Parthasarathy Ranganathan, Jichuan Chang, Chandrakant Patel, Trevor Mudge, and Steven Reinhardt

Improving NAND Flash Based Disk Caches, Taeho Kgil, David Roberts, and Trevor Mudge

4:30 – 4:45 Drop off your luggage

4:45 Depart for Tian-an-men Square

6:15 – 9:30 Banquet in the Great Hall of People (Sponsored by Intel Corporation and pre-banquet concert sponsored by VMWare)

Wednesday June 25, 2008

All sessions in Grand Ballroom

8:00-8:30 Breakfast

8:30-9:00 Invited Talk: "*Research and Development of Godson Processors*," *Weiwu Hu – ICT, CAS*

9:00 - 9:15 Short Break (prepare for parallel sessions)

9:15 - 10:45 Session 6 (Parallel Sessions)

Session 6a *Reliability*

Chair: *Weimin Zheng, Tsinghua University*

Online Estimation of Architectural Vulnerability Factor for Soft Errors, Xiaodong Li, Sarita V. Adve, Pradip Bose, and Jude A. Rivers

A Proactive Wearout Recovery Approach for Exploiting Microarchitectural Redundancy to Extend Cache SRAM Lifetime, Jeonghee Shin, Victor Zyuban, Pradip Bose, and Timothy M. Pinkston

Variation-Aware Application Scheduling and Power Management for Chip Multiprocessors, Radu Teodorescu and Josep Torrellas

Session 6b *Application Acceleration*

Chair: *Luis Ceze, University of Washington*

Flexible Hardware Acceleration for Instruction-Grain Program Monitoring, Shimin Chen, Michael Kozuch, Theodoros Strigkos, Babak Falsafi, Phillip B. Gibbons, Todd C. Mowry, Viyaya Ramachandran, Olatunji Ruwase, Michael Ryan, and Evangelos Vlachos

VEAL: Virtualized Execution Accelerator for Loops, Nathan Clark, Amir Hormati, and Scott Mahlke

From Speculation to Security: Practical and Efficient Information Flow Tracking Using Speculative Hardware, Haibo Chen, Xi Wu, Liwei Yuan, Binyu Zang, Pen-chung Yew, and Frederic T. Chong

10:45 - 11:00 Break 4

11:00 - 12:00 Session 7 (Parallel Sessions)

Session 7a *Performance Evaluation*

Chair: *Josep Torrellas, UIUC*

Software-Controlled Priority Characterization of POWER5 Processor, Carlos Boneti, Francisco J. Cazorla, Roberto Gioiosa, Alper Buyuktosunoglu, Chen-Yong Cher, and Mateo Valero

Learning and Leveraging the Relationship between Architecture-Level Measurements and Individual User Satisfaction, *Alex Shye, Berkin Ozisikyilmaz, Arindam Mallik,* Gokhan Memik, Peter A. Dinda, Robert P. Dick, and Alok N. Choudhary

Session 7b *Multi-core/Many-core Design*

Chair: *Xuejun Yang, NUDT*

Atomic Vector Operations on Chip Multiprocessors, Sanjeev Kumar, Daehyun Kim, Mikhail Smelyanskiy, Yen-Kuang Chen, Jatin Chhugani, Christopher J. Hughes, Changkyu Kim, Victor W. Lee, and Anthony D. Nguyen

3D-Stacked Memory Architectures for Multi-Core Processors, Gabriel H. Loh

12:00 Closing

12:15 Departure for the Great Wall

12:15–5:30 Great Wall Excursion (Sponsored by HP**)**

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