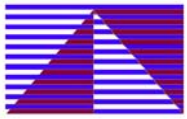
33rd International Symposium on Computer Architecture



June 17-21, 2006
Boston Park Plaza Hotel
Boston, MA

Final Program

Monday June 19, 2006

8:00-8:30 – Breakfast
8:30-8:40 – Welcome
8:40-9:40 – Keynote 1 –

Computer Architecture Research and Future Microprocessors: Where do we go from here?
Yale Patt, University of Texas
Chair: Mateo Valero, *UPC and BSC*

9:40-10:40 – Session 1 – ***Interconnection Networks***
Chair: Wen-Mei W. Hwu, *University of Illionis at Urbana-Champaign*

- *A Gracefully Degrading and Energy-Efficient Modular Router Architecture for On-Chip Networks*, Jongman Kim (Penn State), Chrysostomos A. Nicopoulos (Penn State), Dongkook Park (Penn State), N. Vijaykrishnan (Penn State), Mazin S. Yousif (Intel Corporation), Chita R. Das (Penn State)

- *The BlackWidow High-Radix Clos Network,* Steve Scott (Cray), Dennis Abts (Cray), John Kim (Stanford University), Bill Dally (Stanford University)

10:40-11:00 – Break 1
11:00-12:30 – Session 2 – ***Memory Models***
Chair: José F. Martínez, *Cornell University*

- *Memory Model = Instruction Reordering + Store Atomicity*, Arvind (MIT), Jan Willem Maessen (Sun Microsystems)

- *Conditional Memory Ordering*, Christoph von Praun, Harold W. Cain, Jong-Deok Choi , Kyung Dong Ryu (IBM T.J. Watson Research Center)

- *Architectural Semantics for Practical Transactional Memory*, Austen McDonald, Stanford, JaeWoong Chung, Brian D. Carlstrom, Chi Cao Minh, Hassan Chafi, Christos Kozyrakis, Kunle Olukotun (Stanford University)

12:30 – 2:00 – Monday Lunch
2:00-3:30 – Session 3 – ***Power and Thermal Management***
Chair: Josep Torrellas, *University of Illionis at Urbana-Champaign*

- *Ensemble-level Power Management for Dense Blade Servers*, Parthasarathy Ranganathan (HP Labs), Phil Leech (HP Labs), David Irwin (Duke University), Jeff Chase (Duke University)

- *Techniques for Multicore Thermal Management: Classification and New Exploration*, James Donald, Margaret Martonosi (Princeton University)

- *SODA: A Low-power Architecture for Software Radio*, Yuan Lin (University of Michigan), Hyunseok Lee (University of Michigan), Marh Woh (University of Michigan), Yoav Harel

(University of Michigan), Scott Mahlke (University of Michigan), Trevor Mudge (University of Michigan), Chaitali Chakrabarti (Arizona State University), Krisztián Flautner (ARM)

3:30-4:00 – Break 2

4:00-5:00 – Session 4 – ***Multicore***

Chair: Bill Dally, *Stanford University*

- *An Integrated Framework for Dependable and Revivable Architecture Using Multicore Processors*, Weidong Shi (Georgia Tech), Hsien-Hsin S. Lee (Georgia Tech), Laura Falk (University of Michigan), Mrinmoy Ghosh (Georgia Tech)

- *Multiple Instruction Stream Processor*, Richard A. Hankins (Intel), Gautham N. Chinya (Intel), Jamison D. Collins (Intel), Perry H. Wang (Intel), Ryan Rakvic (United States Naval Academy), Hong Wang (Intel), John P. Shen (Intel)

5:00-6:30 – Panel Session "System 2020: Computer Architecture Grand Research Challenges"
Mary Jane Irwin (Penn State), David Patterson (UC-Berkeley), John P. Shen (Intel)

6:30-7:30 – SIGARCH/TCCA Meeting

Tuesday June 20, 2006

8:00-8:30 – Breakfast

8:30-9:30 – Keynote 2 –

The End of Scaling? Revolutions in Technology and Microarchitecture as we pass the 90 Nanometer Node

Philip Emma – IBM T. J. Watson Research Center

Chair: Per Stenstrom

9:30-10:30 – Session 5 (parallel session)

Session 5A – ***Memory Access Issues***

Chair: Antonio González, *UPC and Intel Corp.*

- *Design and Management of 3D Chip Multiprocessors using Network-in-Memory,*
  Feihui Li, Chrys Nicopoulos, Tom Richardson, Yuan Xie, Narayanan Vijaykrishnan, Mahmut Kandemir (Penn State)

- *Slackened Memory Dependence Enforcement: Combining Opportunistic Forwarding with Decoupled Verification*, Alok Garg, M. Wasiur Rashid, Michael Huang (University of Rochester)

Session 5B – ***Cache Design I***

Chair: Ronny Ronen, *Intel Corp.*

- *Balanced-Cache: Reducing Conflict Misses of Direct-Mapped Caches through Programmable Decoders*, Chuanjun Zhang, (University of Missouri-Kansas City)

- *A Case for MLP-Aware Cache Replacement*, Moinuddin K. Qureshi, Daniel N. Lynch, Onur Mutlu, Yale N. Patt, (University of Texas at Austin)

10:30-11:00 – Break 3

11:00-12:30 – Session 6 (parallel session)

Session 6A – ***Security and Network Processors***

Chair: Hsien-Hsin Lee, *Georgia Tech*

- *Improving Cost, Performance, and Security of Memory Encryption and Authentication*, Chenyu Yan (Georgia Tech), Brian Rogers (North Carolina State University), Daniel Englender (Georgia Tech), Yan Solihin (North Carolina State University), Milos Prvulovic (Georgia Tech)

- *A Scalable Architecture for High-Throughput Regular- Expression Pattern Matching*, Benjamin C. Brodie, Ron K. Cytron, David E. Taylor (Exegy)

- *Chisel: A Storage-Efficient, Collision-Free Hash-based Network Processing Architecture,* Jahangir Hasan (Purdue), Srihari Cadambi (NEC), Venkata Jakkula (NEC), Srimat Chakradhar (NEC)

Session 6B - ***Multithreading***

Chair: Susan Eggers, *Unviersity of Washington*

- *Tolerating Dependences Between Large Speculative Threads Via Sub-Threads*, Christopher B. Colohan (Google), Anastassia Ailamaki (CMU), J. Gregory Steffan (University of Toronto), Todd C. Mowry (CMU and Intel Research Pittsburgh)

- *Bulk Disambiguation of Speculative Threads in Multiprocessors*, Luis Ceze (University of Illinois), James Tuck (University of Illinois), Calin Cascaval (IBM Research), Josep Torrellas (University of Illinois)

- *Learning-Based SMT Processor Resource Distribution via Hill-Climbing*, Seungryul Choi, Donald Yeung (University of Maryland)

12:30-2:30 – Awards Lunch

2:30-3:30 – Session 7 (parallel session)

Session 7A – ***Cache Design II***

Chair: Kei Hiraki, *University of Tokyo*

- *Spatial Memory Streaming*, Stephen Somogyi (Carnegie Mellon University), Thomas F. Wenisch (Carnegie Mellon University), Anastassia Ailamaki (Carnegie Mellon University), Babak Falsafi (Carnegie Mellon University), Andreas Moshovos (University of Toronto)

- *Cooperative Caching for Chip Multiprocessors*, Jichuan Chang, Gurindar S. Sohi, (University of Wisconsin)

Session 7B - ***Potpourri***

Chair: Daniel Jiménez, *Rutgers University*

- *Reducing Startup Time in Co-Designed Virtual Machines*, Shiliang Hu, James E. Smith, (University of Wisconsin)

- *TRAP-Array: A Disk Array Architecture Providing Timely Recovery to Any Point-in-time*, Qing Yang, Wijun Xiao, Jin Ren, (University of Rhode Island)

3:30-4:00 – Break 4

4:00-5:00 – Session 8 (parallel session)

Session 8A – ***Dataflow***

Chair: Yale Patt, *University of Texas at Austin*

- *Program Demultiplexing: Data-flow Execution of Methods in Sequential Programs*, Saisanthosh Balakrishnan, Gurindar S. Sohi, (University of Wisconsin)

- *Area-Performance Trade-offs in Tiled Dataflow Architectures*, Steven Swanson, Andrew Putnam, Martha Mercaldi, Ken Michelson, Andrew Petersen, Andrew Schwerin, Mark Oskin, Susan Eggers, (University of Washington)

Session 8B – ***Cache Coherence***

Chair: Alex Veidenbaum, *University of California Irvine*

- *Flexible Snooping: Adaptive Forwarding and Filtering of Snoops in Embedded-Ring Multiprocessors*, Karin Strauss (University of Illinois), Xiaowei Shen (IBM Research), Josep Torrellas (University of Illinois)

- *Interconnect-Aware Coherence Protocols for Chip Multiprocessors*, Liqun Cheng, Naveen Muralimanohar, Karthik Ramani, Rajeev Balasubramonian, John B. Carter (University of Utah)

5:30–10:00 – Excursion – Odyssey Cruise on Boston Harbor

Wednesday June 21, 2006

8:30-9:00 – Breakfast

9:00-10:00 – Keynote 3 –

The Future of Virtualization Technology

Steve Herrod, VMware

Chair: David Kaeli, *Northeastern University*

10:00-10:30 – Break 5

10:30-12:00 – Session 9 – ***Quantum Computing***

Chair: Matthew Farrens, *University of California-Davis*

- *Distributed Arithmetic on a Quantum Multicomputer*, Rodney Van Meter (Keio University), W. J. Munro (HP Labs), Kae Nemoto (NII), Kohei M. Itoh (Keio University)

- *Interconnection Networks for Scalable Quantum Computers*, Nemanja Isailovic, Yatish Patel, Mark Whitney, John Kubiatowicz (UC Berkeley)

- *Quantum Memory Hierarchies: Efficient Designs to Match Available Parallelism in Quantum Computing*, Darshan D. Thaker (UC Davis), Tzvetan S. Metodi (UC Davis), Andrew W. Cross (MIT), Isaac L. Chuang (MIT), Frederic T. Chong (UC Santa Barbara)

12:00 – Closing

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